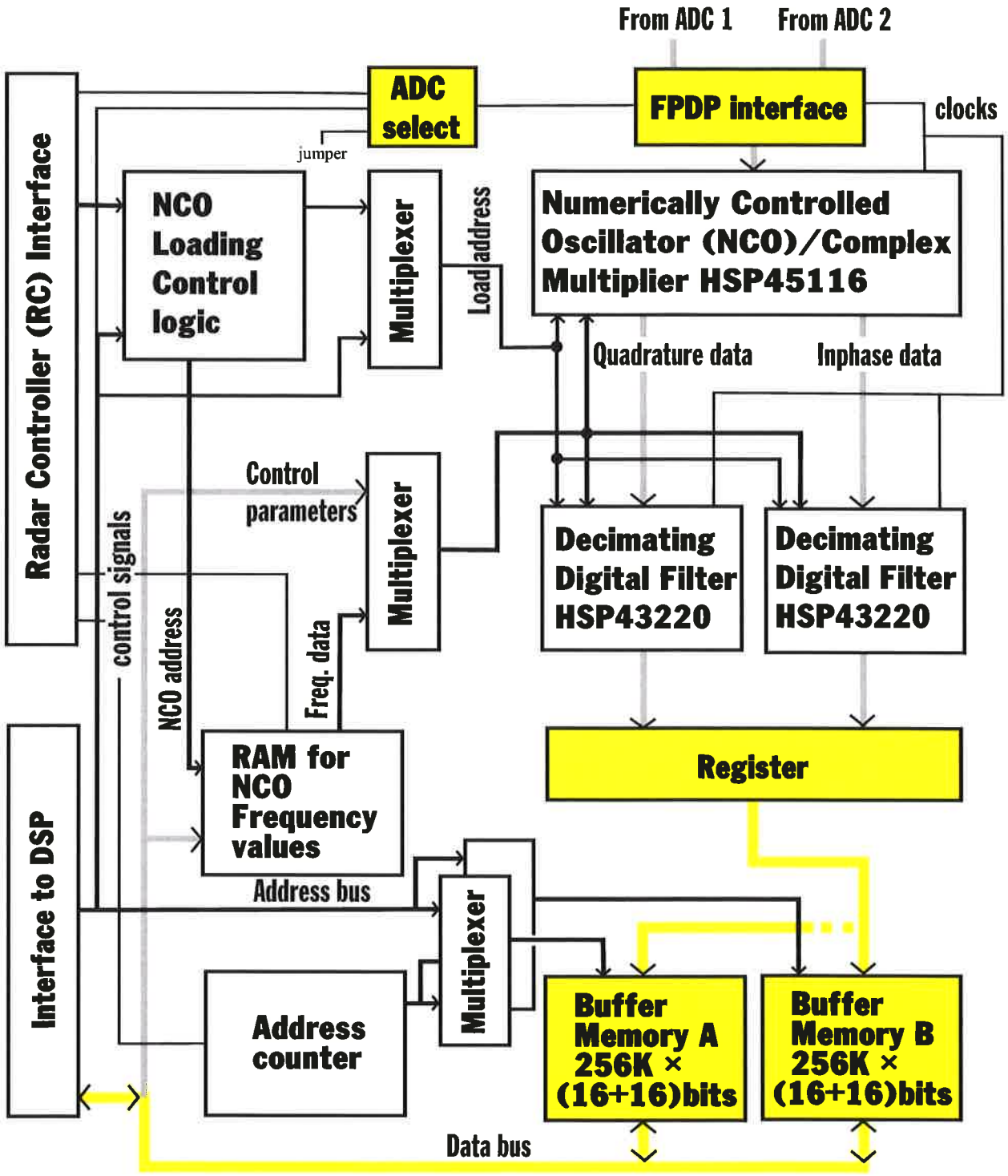
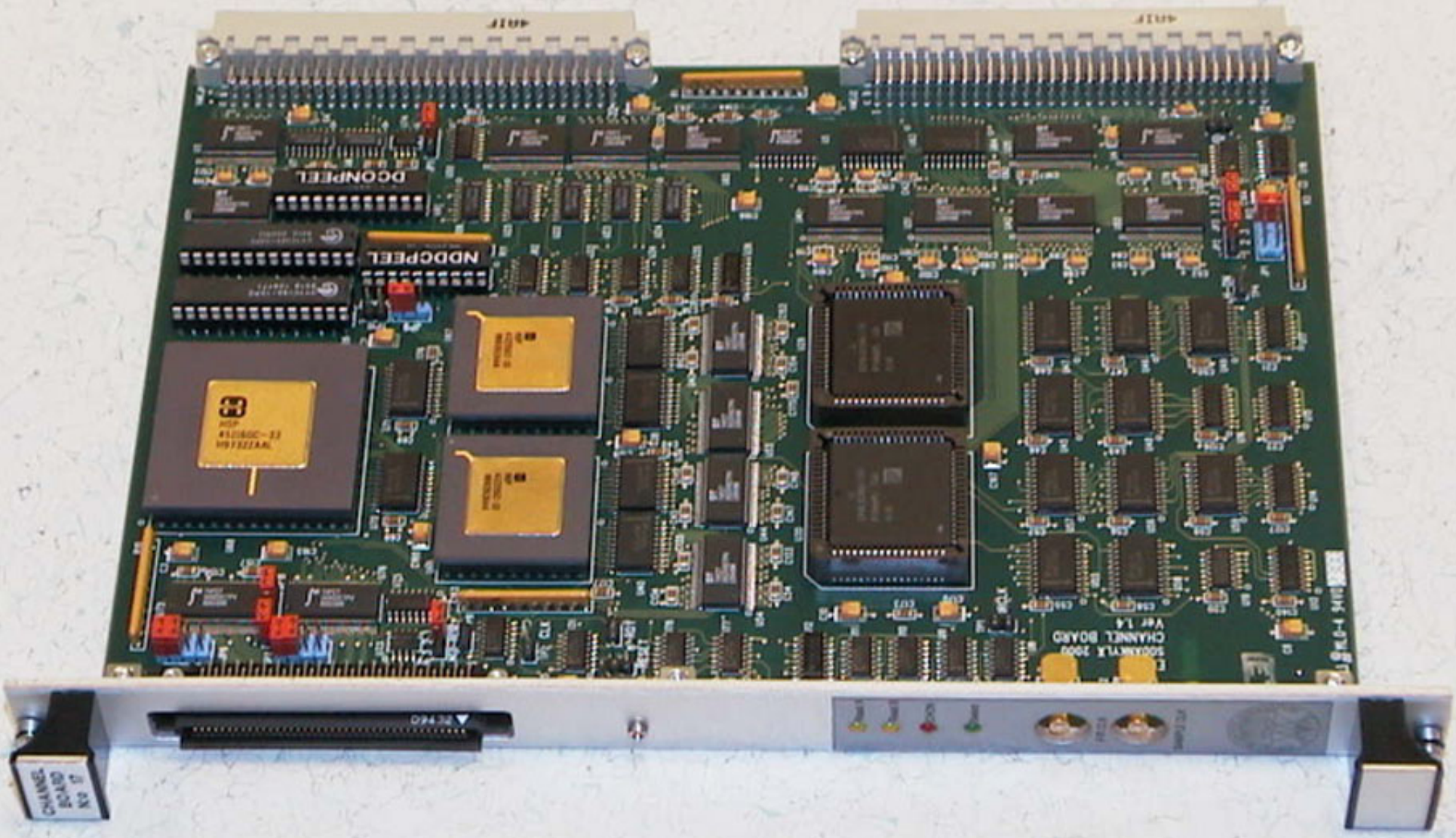

From ADC 1
From ADC 2
ADC select
FPDP interface
clocks
jumper
Radar Controller (RC) Interface
NCO Loading Control logic
Multiplexer
Load address
Numerically Controlled Oscillator (NCO)/Complex Multiplier HSP45116
Quadrature data
Inphase data
Control parameters
Multiplexer
Decimating Digital Filter HSP43220
Decimating Digital Filter HSP43220
control signals
NCO address
Freq. data
RAM for NCO Frequency values
Register
Interface to DSP
Address bus
Multiplexer
Address counter
Buffer Memory A 256K × (16+16)bits
Buffer Memory B 256K × (16+16)bits
Data bus


4MIF
4MIF
DCONPEEL
NDDCPEEL
CHANNEL BOARD
Ver 1.4

Channel board versions

Ver. 1.0 ESR wirewrapped proto (Mixer & filter board), 1994

Ver. 1.1 ESR Printed Circuit Board, 1995

Ver. 1.2 KST proto (PCB), 12/1999

Differences to Ver 1.1

- 32bit wide data busses, 4 times more buffer memory, FPDP interface to the ADC

Ver. 1.3 , 4/2000

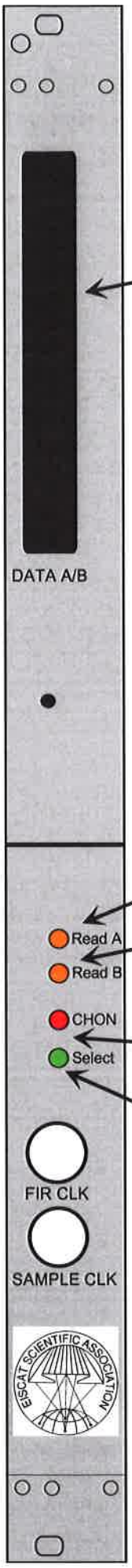
Differences to Ver 1.2

- (NCO) loading is phase-locked to (30 MHz) , better decoupling capacitors of the data tranceivers, I/O-function 7H (Read the status register) changed to 8H and I/O-function FH (Reset) changed to 9H.

Ver. 1.4 6/2000

Differences to Ver 1.3

- ADC select is possible from the RC or from the control SW



Front Panel Data Port (FPDP) connector (ADC1- and ADC2- data + sample clock)

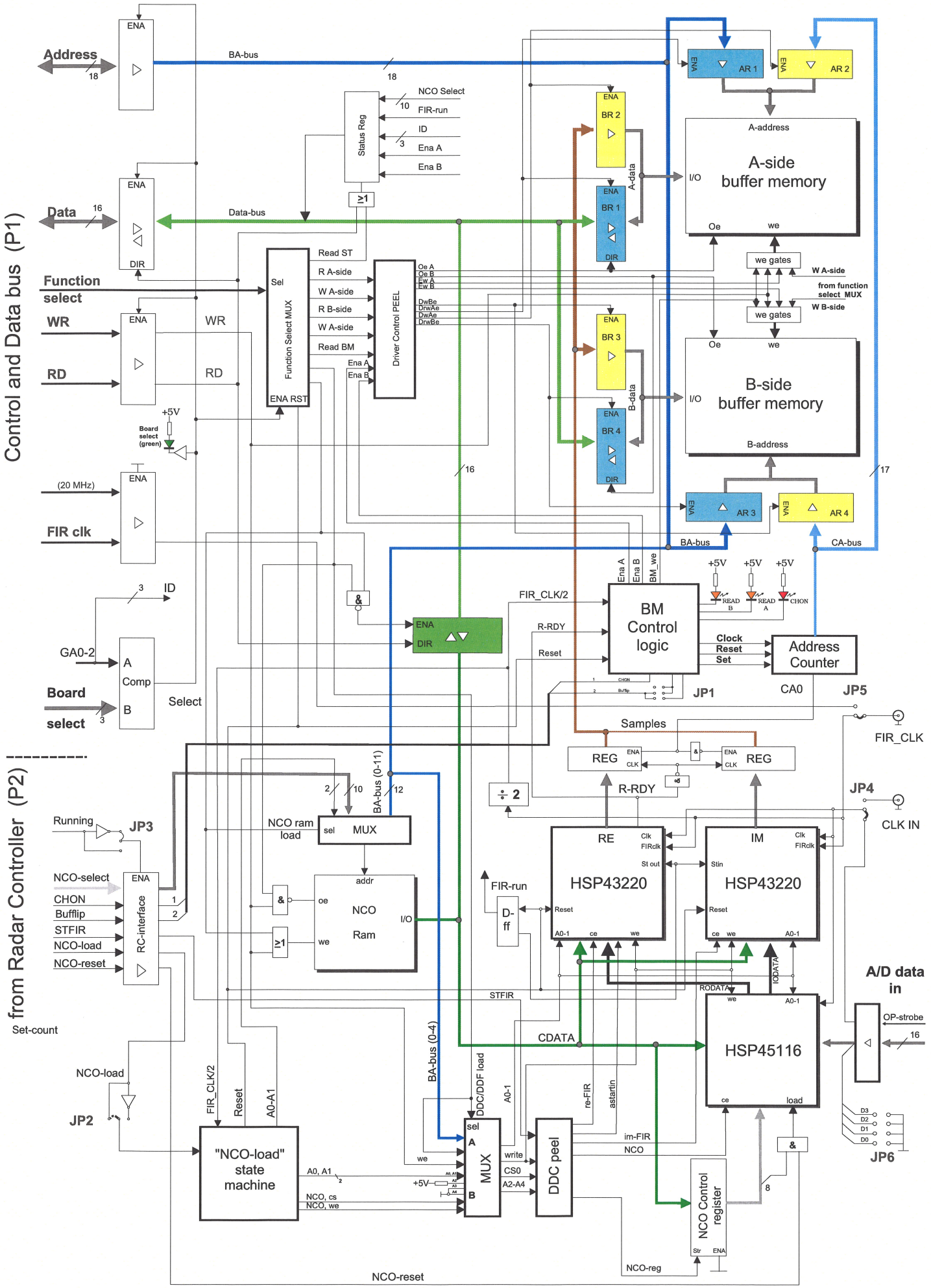
Light, when the RC has released the A-side buffer memory for VME read

Light, when the RC has released the B-side buffer memory for VME read

Light, when the sample gate is opened!

Light, when the board is selected for read, write, loading etc. from the VME

G:\hardwork\kstradar\documents\chfrleds.ds4


Control and Data bus (P1)
from Radar Controller (P2)
Address
18
BA-bus
ENA
AR 1
AR 2
NCO Select
10
FIR-run
ID
3
Ena A
Ena B
Status Reg
≥1
BR 2
BR 1
BR 3
BR 4
DIR
A-data
B-data
A-address
A-side buffer memory
B-side buffer memory
B-address
I/O
Oe
we
we gates
W A-side
from function select MUX
W B-side
Data
16
Data-bus
Function select
WR
RD
Sel
Function Select MUX
Read ST
R A-side
W A-side
R B-side
W A-side
Read BM
Ena A
Ena B
ENA RST
Driver Control PEEL
Oe A
Oe B
Ew A
Ew B
DwBe
DrwAe
DwAe
DrwBe
+5V
Board select (green)
(20 MHz)
FIR clk
17
BA-bus
CA-bus
Ena A
Ena B
BM_we
READ B
READ A
CHON
BM Control logic
FIR_CLK/2
R-RDY
Reset
Clock
Reset
Set
Address Counter
CA0
JP1
JP5
FIR_CLK
ID
GA0-2
Board select
A
Comp
B
Select
Samples
REG
CLK
÷ 2
JP4
CLK IN
Running
JP3
NCO-select
CHON
Bufflip
STFIR
NCO-load
NCO-reset
RC-interface
NCO ram load
MUX
BA-bus (0-11)
addr
NCO Ram
oe
we
I/O
RE
IM
HSP43220
Clk
FIRclk
St out
Stin
Reset
ce
A0-1
FIR-run
D-ff
STFIR
RODATA
IODATA
A/D data in
OP-strobe
HSP45116
CDATA
load
Set-count
NCO-load
JP2
FIR_CLK/2
Reset
A0-A1
"NCO-load" state machine
BA-bus (0-4)
DDC/DDF load
sel
A
B
MUX
write
CS0
A2-A4
DDC peel
re-FIR
astartin
im-FIR
NCO
A0, A1
+5V
NCO, cs
NCO, we
NCO Control register
Str
ENA
NCO-reg
NCO-reset
D3
D2
D1
D0
JP6

JP6 (The size of AD1 data output word)

7-8	X	-	-	-	-
5-6	X	X	-	-	-
3-4	X	X	X	-	-
1-2	X	X	X	X	-

12 bit ADC, 13 bit ADC, 14 bit ADC, 15 bit ADC, 16 bit ADC

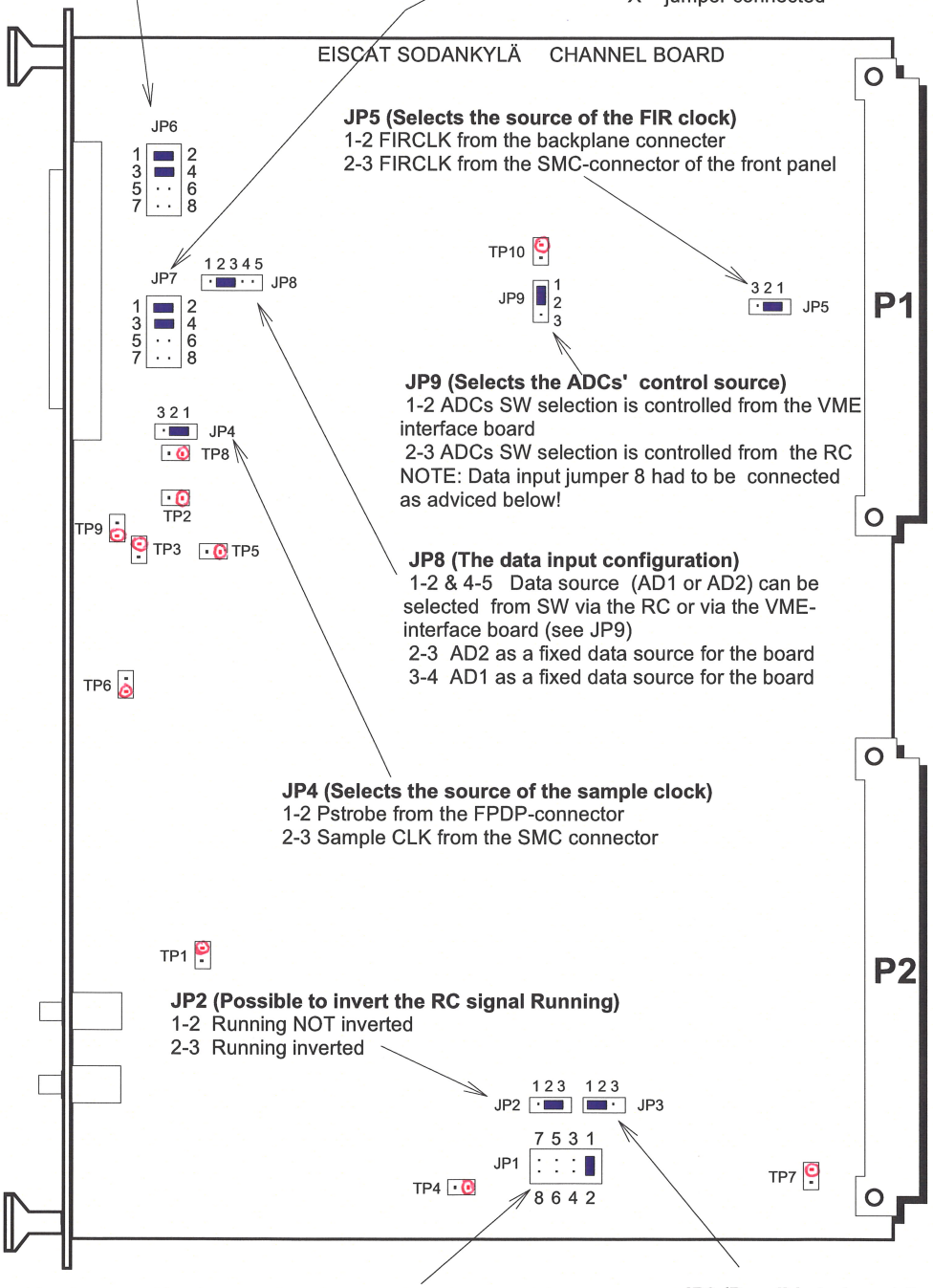
X = jumper connected

JP7 (The size of AD2 data output word)

7-8	X	-	-	-	-
5-6	X	X	-	-	-
3-4	X	X	X	-	-
1-2	X	X	X	X	-

12 bit ADC, 13 bit ADC, 14 bit ADC, 15 bit ADC, 16 bit ADC

X = jumper connected



JP5 (Selects the source of the FIR clock)
1-2 FIRCLK from the backplane connecter
2-3 FIRCLK from the SMC-connector of the front panel

JP9 (Selects the ADCs' control source)
1-2 ADCs SW selection is controlled from the VME interface board
2-3 ADCs SW selection is controlled from the RC
NOTE: Data input jumper 8 had to be connected as adviced below!

JP8 (The data input configuration)
1-2 & 4-5 Data source (AD1 or AD2) can be selected from SW via the RC or via the VME-interface board (see JP9)
2-3 AD2 as a fixed data source for the board
3-4 AD1 as a fixed data source for the board

JP4 (Selects the source of the sample clock)
1-2 Pstrobe from the FPDP-connector
2-3 Sample CLK from the SMC connector

JP2 (Possible to invert the RC signal Running)
1-2 Running NOT inverted
2-3 Running inverted

Test Points (always pair: active signal + GND)
TP1 = FIRCLK
TP2 = CLK_in
TP3 = Reset
TP4 = CHON
TP5 = R-RDY
TP6 = WR
TP7 = RD
TP8 = NC0-reset
TP9 = NCO-load
TP10 = Astart

JP1 (Possible select the sources of the address counter Load and Clear signals)
7-8 Not in use
5-6 RC STFIR connected to the address counter Load
3-4 RC Bufflip connected to the address counter Load
1-2 RC Bufflip connected to the address counter Clear

JP3 (Possible to invert the RC signal NCO-Load)
1-2 NCO-Load NOT inverted
2-3 NCO-Load inverted

= Default settings